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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,318	HABA, BELGACEM	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) *10, 14, 15, 34, 36, 37 and 55* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 11-13, 16-33, 35, 38-54 and 56-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/27/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Embodiment 1 of figs. 1-7 and 12-14 in the reply filed on April 17, 2006 is acknowledged. Claims 1-9, 11-13, 16-33, 35, 38-54 and 56-59 are readable upon the elected species of Embodiment 1. Thereby claims 10, 14, 15, 34, 36, 37, and 55 are withdrawn from further consideration.

Claim Objections

2. Claim 50 is objected to because of a lack of antecedent basis. The claim recites the limitation "the at least one bend" in lines 1-2 of claim 50. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-9, 11-13, 16-24, 32, 33, and 53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation, "in a generally downward direction," in line 4 of claim 1, is unclear and indistinct, because the limitation has multiple interpretations. Does the limitation, "at least one offset portion offset from the attachment portion in a generally downward direction," mean that the whole offset portion or part of the offset portion is in a

downward direction? What is the scope of the limitation, "generally downward direction," in claim 1? The office will interpret "generally downward direction" to mean that a part of the offset portion is in a downward direction. Claims 2-9, 11-13 and 16-24, are dependent on claim 1, and thus are also rejected.

The limitation, "generally downwardly," in line 4 of claim 8, is unclear and indistinct, because the limitation has multiple interpretations. Does the limitation, "the offset portion of the dielectric layer extends generally downwardly," mean that the whole offset portion or part of the offset portion extends generally downwardly? What is the scope of the limitation, "generally downwardly," in claim 4?

The limitation, "generally horizontally," in line 2 of claim 13, is unclear and indistinct, because the limitation has multiple interpretations. Does the limitation, "wherein the at least one outer end extends generally horizontally," mean that all of the outer end or part of the outer end extends generally horizontally? What is the scope of the limitation, "generally horizontally," in claim 13?

The limitation, "generally downwardly," in line 4 of claim 32, is unclear and indistinct, because the limitation has multiple interpretations. Does the limitation, "the outer ends of the dielectric layer extend generally downwardly," mean that all of the outer ends or part of the outer ends extends generally downwardly? What is the scope of the limitation, "generally downwardly" in claim 32?

The limitation, "generally horizontally," in line 2 of claim 33, is unclear and indistinct, because the limitation has multiple interpretations. Does the limitation, "wherein the outer ends of the dielectric layer extend generally horizontally," mean that

all of the outer ends or part of the outer ends extended generally horizontally? What is the scope of the limitation, "generally horizontally" in claim 33?

The limitations, "generally horizontal" and "generally extends downwardly," in lines 2-3 of claim 53, are unclear and indistinct, because the limitations have multiple interpretations. Is the whole attachment portion or part of the attachment portion horizontal? Does the whole offset portion or part of the offset extend downwardly? What is the scope of the limitations, "generally horizontal" and "generally extends downwardly," in claim 53?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-9, 11-13, 16-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Appelt et al. (5,900,675).

With respect to claim 1, Appelt teaches a microelectronic assembly, comprising:

a) a dielectric layer **505** having an attachment portion, the dielectric layer having at least one offset portion offset from the attachment portion in a generally downward direction (as best interpreted by the office) (fig. 5);

b) a semiconductor chip **520** assembled to the attachment portion; and

c) terminal structures **550** carried by the offset portion of the dielectric layer **505** for connecting the semiconductor chip **520** with external circuitry lying at a lower level than the attachment portion (fig. 5, col. 5, lns. 42-56).

With respect to claim 2, Appelt teaches the assembly of claim 1 as set forth above, wherein the attachment portion of the dielectric layer **505** is generally planar (fig. 5).

With respect to claim 3, Appelt teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **505** has at least one bend in the dielectric layer between the attachment portion and the offset portion (fig. 5).

With respect to claim 4, Appelt teaches the assembly of claims 1 and 3 as set forth above, wherein the at least one bend comprises a first bend in a first direction and a second bend in a second direction opposite to the first direction (fig. 5).

With respect to claim 5, Appelt teaches the assembly of claims 1, 3, and 4 as set forth above, wherein the dielectric layer **505** has at least one conductor **515** extending in the bend (fig. 5).

With respect to claim 6, Appelt teaches the assembly of claims 1, 3, 4, and 5 as set forth above, wherein the at least one conductor **515** is arranged so as to support the bend in the dielectric layer (fig. 5).

With respect to claim 8, Appelt teaches the assembly of claim 1 as set forth above, wherein the semiconductor chip **520** is attached to the dielectric layer **505** at a bottom surface of the dielectric layer and the offset portion of the dielectric layer extends

generally downwardly (as best interpreted by the office) alongside the semiconductor chip (fig. 5).

With respect to claim 9, Appelt teaches the assembly of claims 1 and 8 as set forth above, wherein the dielectric layer **505** has at least one conductor **510 and 515**, arranged so as to shield the semiconductor chip (fig. 5).

With respect to claim 11, Appelt teaches the assembly of claim 1 as set forth above, wherein the offset portion of the dielectric layer **505** comprises a portion that lies outwardly of the attachment portion of the dielectric layer (fig. 5).

With respect to claim 12, Appelt teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **505** has at least one outer end and the terminal structures **550** are disposed at the at least one outer end (fig. 5).

With respect to claim 13, Appelt teaches the assembly of claims 1 and 12 as set forth above, wherein the at least one outer end extends generally horizontally (as best interpreted by the office) (fig. 5).

With respect to claim 16, Appelt teaches the assembly of claim 1 as set forth above, further comprising a circuit element **560** connected to the terminal structures **550** so that the circuit element is disposed underneath the dielectric layer **505** (fig. 5).

With respect to claim 17, Appelt teaches the assembly of claims 1 and 16 as set forth above, wherein the terminal structures **550** interconnect the semiconductor chip **520** with the circuit element **560** (fig. 5).

With respect to claim 18, Appelt teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **505** includes traces **515** connected to the terminal structures **550** and connected to contacts **525** of the semiconductor chip **520** (fig. 5).

With respect to claim 19, Appelt teaches the assembly of claim 1 as set forth above, wherein the semiconductor chip **520** has a first face with contacts **525** exposed at the first face (fig. 5).

With respect to claim 20, Appelt teaches the assembly of claims 1 and 19 as set forth above, wherein the semiconductor chip **520** is assembled to the attachment portion so that the first face faces in an upward direction (fig. 5).

With respect to claim 21, Appelt teaches the assembly of claim 1 as set forth above, wherein the dielectric layer **505** comprises a continuous sheet (fig. 5).

With respect to claim 22, Appelt teaches the assembly of claim 1 as set forth above, wherein the terminal structures **550** comprise bonding material ("BGA solder balls," col. 5, lns. 49-50).

With respect to claim 24, Appelt teaches the assembly of claim 1 as set forth above, wherein the terminal structures **550** comprise solder balls (col. 5, lns. 49-50).

With respect to claim 25, Appelt teaches a microelectronic assembly, comprising:

a) a dielectric layer **505** having an attachment portion, the dielectric layer having outer ends lying outwardly of the attachment portion, the outer ends being offset from the attachment portion (fig. 5);

b) a semiconductor chip **520** assembled to the attachment portion; and

c) terminal structures **550** carried by the outer ends of the dielectric layer **505** for connecting the semiconductor chip with external circuitry (fig. 5, col. 5, lns. 42-56).

With respect to claim 26, Appelt teaches the assembly of claim 25 as set forth above, wherein the attachment portion of the dielectric layer **505** is generally planar (fig. 5).

With respect to claim 27, Appelt teaches the assembly of claim 25 as set forth above, wherein the outer ends extend downwardly alongside the semiconductor chip **520** and have at least one conductor **510 and 515**, arranged so as to shield the semiconductor chip (fig. 5).

With respect to claim 28, Appelt teaches the assembly of claim 25 as set forth above, wherein the dielectric layer **505** has at least one bend in the dielectric layer between the attachment portion and the outer ends (fig. 5).

With respect to claim 29, Appelt teaches the assembly of claims 25 and 28 as set forth above, wherein the at least one bend comprises a first bend in a first direction and a second bend in a second direction opposite to the first direction (fig. 5).

With respect to claim 30, Appelt teaches the assembly of claims 25 and 28 as set forth above, wherein the dielectric layer has at least one conductor **515** extending in the bend (fig. 5).

With respect to claim 31, Appelt teaches the assembly of claims 25, 28 and 30 as set forth above, wherein the at least one conductor **515** is arranged so as to support the bend in the dielectric layer (fig. 5).

With respect to claim 32, Appelt teaches the assembly of claim 25 as set forth above, wherein the semiconductor chip **520** is attached to the dielectric layer **505** at a bottom surface of the dielectric layer **505** and the outer ends of the dielectric layer extend generally downwardly (as best interpreted by the office) alongside the semiconductor chip **520** (fig. 5).

With respect to claim 33, Appelt teaches the assembly of claim 25 as set forth above, wherein the outer ends of the dielectric layer **505** extend generally horizontally (as best interpreted by the office) (fig. 5).

With respect to claim 35, Appelt teaches the assembly of claim 25 as set forth above, wherein the outer ends lie outwardly of the attachment portion of the dielectric layer (fig. 5).

With respect to claim 38, Appelt teaches the assembly of claim 25 as set forth above, further comprising a circuit element **560** connected to the terminal structures **550** so that the circuit element is disposed underneath the dielectric layer **505** (fig. 5).

With respect to claim 39, Appelt teaches the assembly of claims 25 and 38 as set forth above, wherein the terminal structures **550** interconnect the semiconductor chip **520** with the circuit element **560** (fig. 5).

With respect to claim 40, Appelt teaches the assembly of claim 25 as set forth above, wherein the dielectric layer **505** includes traces **515** connected to the terminal structures **550** and connected to contacts **525** of the semiconductor chip **520** (fig. 5).

With respect to claim 41, Appelt teaches the assembly of claim 25 as set forth above, wherein the semiconductor chip **520** has a first face and contacts **525** exposed at the first face (fig. 5).

With respect to claim 42, Appelt teaches the assembly of claim 25 and 41 as set forth above, wherein the semiconductor chip **520** is assembled to the attachment portion so that the first face faces in an upward direction (fig. 5).

With respect to claim 43, Appelt teaches the assembly of claim 25 as set forth above, wherein the dielectric layer **505** comprises a continuous sheet (fig. 5).

With respect to claim 44, Appelt teaches the assembly of claim 25 as set forth above, wherein the terminal structures **550** comprise bonding material ("BGA solder balls," col. 5, lns. 49-50).

With respect to claim 46, Appelt teaches the assembly of claim 25 as set forth above, wherein the terminal structures **550** comprise solder balls (col. 5, lns. 49-50).

With respect to claim 47, Appelt teaches a microelectronic component, comprising:

a) a dielectric layer **505** comprising a continuous sheet having an attachment portion for assembly with a microelectronic element **520** and an offset portion offset from the attachment portion;

b) terminal structures **550** on the dielectric layer **505**; and

c) conductors **515** attached to the terminal structures **555** (fig. 5, col. 5, lns. 42-56).

With respect to claim 48, Appelt teaches the component of claim 47 as set forth above, wherein the terminal structures include bonding material ("BGA solder balls," col. 5, lns. 49-50).

With respect to claim 49, Appelt teaches the component of claim 47 as set forth above, wherein the dielectric layer **505** includes at least one bend between the attachment portion and the offset portion (fig. 5).

With respect to claim 50, Appelt teaches the component of claim 47 as set forth above, wherein the at least one bend comprises a first bend in a first direction and a second bend in a second direction opposite the first direction (fig. 5).

With respect to claim 51, Appelt teaches the component of claim 47 as set forth above, wherein the conductors **515** comprise a plurality of traces (fig. 5).

With respect to claim 52, Appelt teaches the component of claims 47 and 51 as set forth above, wherein at least one of the traces **515** is disposed in the bend (fig. 5).

With respect to claim 53, Appelt teaches the component of claim 47 as set forth above, wherein the attachment portion is generally horizontal and the offset portion generally extends downwardly (as best interpreted by the office) (fig. 5).

With respect to claim 54, Appelt teaches the component of claim 47 as set forth above, wherein the offset portion lies outwardly of the attachment portion (fig. 5).

With respect to claim 58, Appelt teaches the component of claim 47 as set forth above, wherein the terminal structures **550** comprise bonding materials ("BGA solder balls," col. 5, lns. 49-50).

With respect to claim 59, Appelt teaches the component of claim 47 as set forth above, wherein the terminal structures **550** comprise solder balls (col. 5, lns. 49-50).

5. Claims 1, 23, 25, and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto (US 6,489,687).

With respect to claim 1, Hashimoto teaches a microelectronic assembly, comprising:

a) a dielectric layer **50** (col. 6, lns. 45-57) having an attachment portion, the dielectric layer having at least one offset portion offset from the attachment portion in a generally downward direction (as best interpreted by the office) (fig. 8);

b) a semiconductor chip **20** assembled to the attachment portion; and

c) terminal structures **90** carried by the offset portion of the dielectric layer **50** for connecting the semiconductor chip **20** with external circuitry lying at a lower level than the attachment portion (fig. 8, col. 8, lns. 40-43).

With respect to claim 23, Hashimoto teaches the assembly of claim 1 as set forth above, wherein the terminal structures **90** are connected to conductors (**14, 16, 18**) extending through **56** the attachment portion (fig. 8, col. 7, lns. 19-24).

With respect to claim 25, Hashimoto teaches a microelectronic assembly, comprising:

a) a dielectric layer **50** having an attachment portion, the dielectric layer having outer ends lying outwardly of the attachment portion, the outer ends being offset from the attachment portion (fig. 8);

b) a semiconductor chip **20** assembled to the attachment portion; and

c) terminal structures **90** carried by the outer ends of the dielectric layer **50** for connecting the semiconductor chip with external circuitry (fig. 8, col. 8, lns. 40-43).

With respect to claim 45, Hashimoto teaches the assembly of claim 25 as set forth above, wherein the terminal structures **90** are connected to conductors (**14, 16, 18**) extending through the attachment portion (fig. 8, col. 7, lns. 19-24).

6. Claims 47 and 57 are rejected under 35 U.S.C. 102(b) as being anticipated by Terui (US 6,472,732).

With respect to claim 47, Terui teaches a microelectronic component, comprising:

a) a dielectric layer **25** (col. 3, lns. 62-64) comprising a continuous sheet having an attachment portion for assembly with a microelectronic element **28** and an offset portion offset from the attachment portion (fig. 8);

b) terminal structures **34** on the dielectric layer **25** (fig. 8); and

c) conductors **23** attached to the terminal structures **34** (fig. 8, col. 4, lns. 32-34).

With respect to claim 57, Terui teaches component of claim 47 as set forth above, wherein the terminal structures include vias **30** defined by the dielectric layer (fig. 8, col. 4, lns. 22-23).

7. Claims 7 and 56 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Appelt ('675) as applied to claims 1 and 47 above, respectively.

With respect to claim 7 and 56, Appelt teaches the microelectronic assembly of claims 1 and 47, respectively, as set forth above, wherein the dielectric layer comprises a polymeric material that includes an offset portion.

As to the grounds of rejection under section 103(a), the method of forming the offset portion by molding the polymeric material is a product by process limitation and therefore is given no patentable.

Initially, and with respect to claims 7 and 56, note that a "product by process" claim is directed to the product per se, no matter how actually made. *In re Thorpe et al.*, 227 USPQ 964, (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product per se which must be determined in a "product by process" claim, and no the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe:

> Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington,* 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935);

Note that Applicant has burden of proof in such cases as the above case law makes it clear.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AK

HOAI PHAM
PRIMARY EXAMINER